Digital Phase Correction for Multiplexed ADCs in Low-Cost Six-Port Interferometers

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***Abstract*— Six-Port based radar systems are often addressing the low-cost metrology market. Currently, the analog-to-digital converter (ADC) is one of the most expensive components as it needs to simultaneously sample the four baseband signals of the Six-Port interferometer. This paper studies the feasibility of digital phase correction techniques to achieve simultaneous sampling with only a single multiplexed ADC in low-cost Six-Port systems. A system demonstrator featuring a low-power 16 bit micro-controller will be shown which compensates the conversion error due to the multiplexing delay with an efficient polyphase implementation leading to a measurement update rate of 2000 distance values per second.**

***Index Terms*— Six-Port, analog-to-digital converter, signal processing, micro-controller.**

I. INTRODUCTION

Originally introduced as an alternative method for vector network analysis [1], the Six-Port receiver has nowadays emerged in a wide variety of different areas. Current applications also include direct conversion communication receivers, e.g., for software defined radio frontends [2] as well as metrology systems, e.g., for high resolution distance and vibration measurement [3]. All of these applications typically require four simultaneous sampling ADCs for optimal system performance. Analog pre-processing could reduce this requirement down to two ADCs, however, for ideal calibration and linearization access to the output of each power detector is required [4].

It has been shown that non-simultaneous sampling leads to a considerable position measurement error in Six-Port based radar systems when the further processing is based on the assumption of ideal synchronization [5]. Even for slow moving targets with a linear movement and a velocity of $v = 1\frac{m}{s}$ the resulting position error is already above 1 mm when using a single ADC with a sampling rate of 1 kSa/s [5]. The same will apply for the bit error rate of communication systems. Thus, correction techniques are required that correct the phase error introduced by the multiplexer in the digital domain with accordingly low computational effort to be implemented on a low-cost micro-controller. Mainly two solutions exist in literature for this problem, one based on multirate techniques [6] and the other on fractional delay filters [7]. This paper will focus on a realization based on multirate systems as the whole process finally breaks down to a lowpass filter design that can be efficiently implemented using polyphase structures. Furthermore they feature a lower computational effort for low oversampling ratios compared to fractional delay Lagrange filters [8].

II. BASEBAND CONCEPT

A. *Six-Port fundamentals*

A simplified block diagram of a Six-Port based radar-system is depicted in Fig. 1. The system measures the phase difference between two coherent signals to provide precise relative distance information between the system and the target.

A voltage controlled oscillator is used to generate a mono-frequent radio frequency (RF) signal. This signal is divided into two equal party by a hybrid coupler. One part is used as reference and is fed to the first input port P_1 of the Six-Port structure. The other part is transmitted by the antenna to the target, partly reflected by this target, finally received by the antenna again and fed to the second input port P_2. Both signals are superimposed under four different relative phase shifts of 0, $\frac{\pi}{2}$, π and $\frac{3\pi}{2}$ in the Six-Port interferometer forming four output signals $P_3 \dots P_6$. Using power detectors these RF signals are directly converted to the DC-voltages $B_3 \dots B_6$. This baseband signals can be

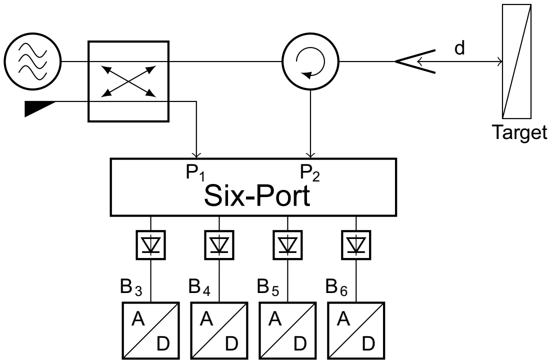


Fig. 1. Simplified block diagramm of a Six-Port based radar system with a conventional baseband [5]

seen as differential I/Q-signals forming the complex vector $\underline{z}$ whose argument equals the phase difference φ between the two input ports.

$$\underline{z} = (B_5 - B_6) + j(B_3 - B_4) \tag{1}$$

$$\varphi = \arg\{\underline{z}\} = \tan^{-1}\left(\frac{\Im(\underline{z})}{\Re(\underline{z})}\right) \tag{2}$$

Knowing the wavelength of the original transmit signal and the measured phase difference φ the relative distance to the target can finally be calculated:

$$d = \frac{\varphi}{2\pi} \cdot \frac{\lambda}{2} \tag{3}$$

B. Conventional Six-Port baseband

A conventional baseband for Six-Port interferometers typically requires its distinct ADC for each baseband channel and the sampling process has to be made simultaneously for ideal system performance. A single or two parallel ADCs can be used, but when the further processing is based on the assumption of ideal synchronization a phase error occurs [5].

Fig. 2 depicts a simulated IQ-diagram for a frequency difference of $f_D = 102\,\mathrm{Hz}$ and $202\,\mathrm{Hz}$ at the Six-Port's inputs sampled with 500 Sa/s. These frequency differences correspond to the Doppler frequency shift (Eq. 4) that a moving target with a constant velocity of $v = 0.64\,\frac{m}{s}$ or $1.26\,\frac{m}{s}$ would create for a 24 GHz radar system.

$$f_D = \frac{2 \cdot v}{\lambda} \tag{4}$$

It can be seen that for multiplexed sampling the IQ-diagram suffers from a frequency dependent distortion, especially when the input signal comes close to the Nyquist frequency.

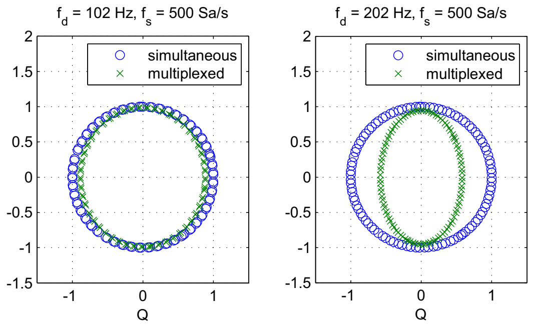


Fig. 2. Simulated IQ-diagram for a difference frequency at the Six-Port's inputs, acquired with simultaneous sampling and multiplexed sampling, respectively

C. Proposed single multiplexed ADC with digital phase correction

The proposed baseband concept is depicted in Fig. 3. It requires just a single ADC with an additional four port analog multiplexer. The sampling of the baseband voltages is made one after another. In the digital domain the data stream gets de-multiplexed and the samples become resynchronized by the concept described in Sec. III. For low-cost operation the whole concept can be realized with a cheap, low-speed micro-controller featuring the ADC.

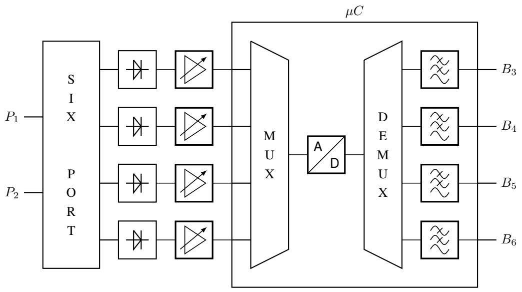
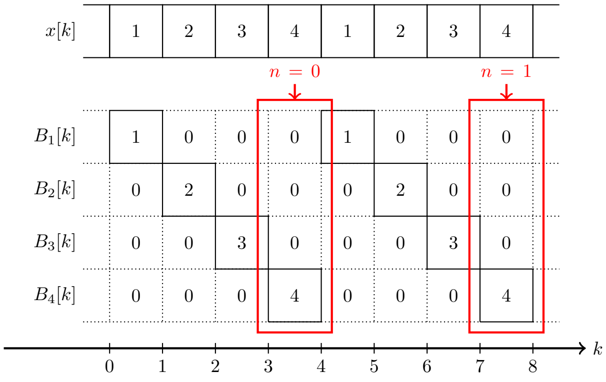


Fig. 3. Block diagram of the proposed single multiplexed ADC baseband with digital phase correction

III. SIGNAL PROCESSING

Due to the multiplexing a per-channel sampling rate of $f_s = \frac{1}{T}$ leads to an overall sampling rate $f_{ADC} = 4\,f_s$ and the output data stream at the ADC $x[k]$ alternately contains the samples of the different baseband channels. When sampling with only one ADC a fractional time delay $\eta_m = \frac{m-4}{4} \cdot T$ is induced to the sampled baseband channels B_m, $m \in \{4, 5, 6, 7\}$. Without compensation in the baseband this results in a non-linear frequency-dependent error in the calculated phase. Due to the fact that η_m is a fraction of T for all m, fractional delay filters can be used to resynchronize the channels [7]. However, the compensation can also be done by directly mapping it onto an upsampled sequence (Fig. 4). The inserted zeros of the upsampled sequence are interpolated by a suitable interpolation filter. As the sampling rate of the formed sequence is four times higher than required for the Nyquist bandwidth, a combination of interpolation and decimation



$x[k]$	1	2	3	4	1	2	3	4
$B_1[k]$	1	0	0	0	1	0	0	0
$B_2[k]$	0	2	0	0	0	2	0	0
$B_3[k]$	0	0	3	0	0	0	3	0
$B_4[k]$	0	0	0	4	0	0	0	4

Fig. 4. Upsampled sequence taking the fractional delay between the baseband channels into account

can be used. For an efficient implementation it is thus sufficient to only calculate every fourth sample during interpolation. The computational effort can be further reduced by calculating only three out of four filters and simply delaying the sequence where $\eta = 0$.

A. *Filter design*

In order to avoid a phase error induced by the interpolation filter, a linear phase filter is required. For an implementation on a low-power micro-controller without a floating-point unit, the limited wordlength needs to be considered as it generates additional noise in the stopband. For the proposed concept, a 220-tab finite impulse response (FIR) filter with an attenuation of 80 dB at the stop band of 1 kHz filter has been designed in MATLAB using the Windowed Fourier Approximation method with a Dolph-Chebyshev window. The magnitude response is depicted in Fig. 5. The dashed line shows the ideal magnitude response with a double precision floating point arithmetic, the continuous line the magnitude response for a 16-bit integer implementation on the mirco-controller.

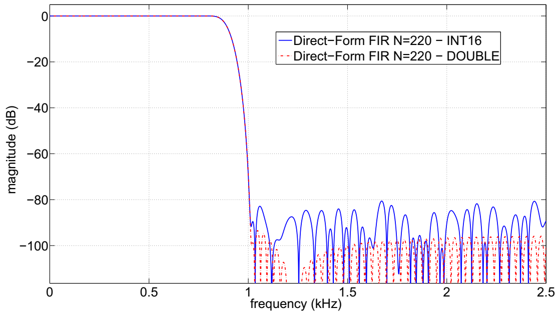


Fig. 5. Magnitude response of the designed low-pass interpolation filter

B. *Efficient polyphase implementation*

By using a polyphase decomposition a FIR filter transfer function H(z) with N coefficients (Eq. 5) can be split into P polyphases with $M = \frac{N}{P}$ coefficients each (Eq. 6).

$$H(z) := \sum_{k=0}^{N-1} h[k] \cdot z^{-k} \tag{5}$$

$$H(z) := \sum_{p=0}^{P-1} \sum_{n=0}^{N-1} h[Pn + p] z^{-Pn} z^{-p} \tag{6}$$

In case of the correction filters $P = 4$ is the ideal choice as three out of four polyphases evaluate to zero when processing the upsampled input data $B_x[k]$. Fig. 6 depicts a block diagram of the decomposed polyphase filters processing an input sequence of $\{x_0, 0, 0, 0, x_0, 0, ...\}$. Only the first polyphase $H_{4,0}(z^4)$ has to be calculated.

Together with the other optimizations the computational effort is drastically reduced by a factor of 21.3 compared to a straight forward implementation.

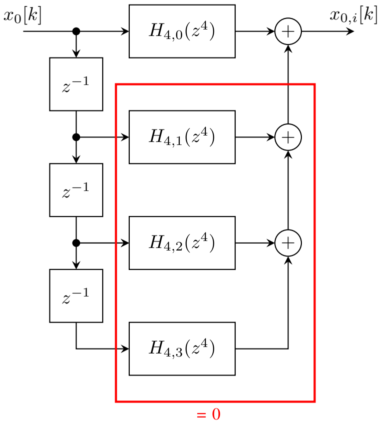


Fig. 6. Interpolating sequence $x_0[k] = \{x_0, 0, 0, 0, x_0, 0, ...\}$ with a polyphase filter. The polyphase components $1-3$ calculate to zero

IV. HARDWARE DESIGN AND EXPERIMENTAL VERIFICATION

A. *Hardware design*

The concept of the single multiplexed ADC has been realized on a printed circuit board (PCB). A photo of the system demonstrator including a 24 GHz Six-Port is depicted in Fig. 7. The 24 GHz Six-Port system, on the right side of the picture, provides the four baseband voltages $B_3 \ldots B_6$ through SMA conncetors to the baseband board, shown on the left side. The core component of the baseband is a MSP430F5529 16-bit micro-controller from Texas Instruments. It features an integrated 12-bit ADC with a sampling rate of up to 200 kSa/s and operates on a main clock rate of 24 MHz. The micro-controller implements the data acquisition and digital filtering for phase correction and can finally send the baseband data through USB to a PC. For a 16-bit fixed-point arithmetic a measurement update rate of 2000 Hz could be achieved (8 kSa/s ADC sampling rate). With a 32-bit arithmetic precision the measurement update rate decreases to 500 Hz (2 kSa/s ADC sampling rate).

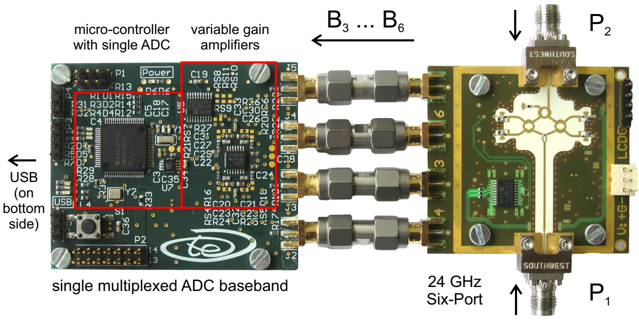
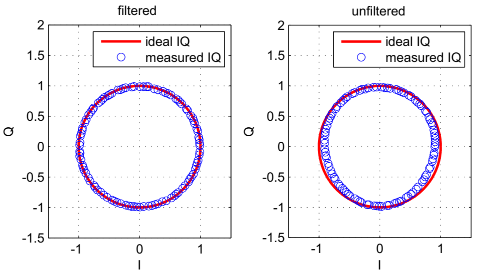


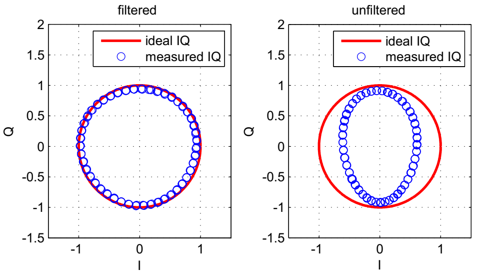
Fig. 7. Photo of a 24 GHz Six-Port interferometer with the single multiplexed ADC baseband

B. *IQ-diagram measurements*

Two synchronized Agilent PSG vector signal generators have been connected to the input ports P_1 and P_2 to emulate a 24 GHz radar system seeing a single target with a Doppler frequency f_d (Eq. 4). The frequency difference was set to 102 Hz and 202 Hz to emulate a slow moving target with a velocity of around $0.64\,\frac{m}{s}$ and $1.26\,\frac{m}{s}$ respectively. In a first measurement with a frequency difference of only 2 Hz the non-idealities of the Six-Port have been compensated according to [9] and the compensation parameters were applied for all further measurements. Fig. 8 depicts the measured IQ-diagrams for each the filtered and unfiltered baseband data. The measurement results show a good agreement with the simulation results (Fig. 2). For the unfiltered measurements there is a strong frequency dependent distortion of the IQ-diagram whereas the filtered results are close to the ideal unit circle. Only for $f_d = 202$ Hz there is a small deviation which arises due to the non-linearities of the power detectors that are now out of the baseband bandwith.



(a) IQ-diagram with $f_d = 102$ Hz, $f_s = 500$ Sa/s



(b) IQ-diagram with $f_d = 202$ Hz, $f_s = 500$ Sa/s

Fig. 8. Measured IQ-diagram with different emulated Doppler shifts for a Six-Port based radar system

V. DISCUSSION

The main benefit of this concept is the reduced hardware requirement in the baseband as a single multiplexed ADC is sufficient. This opens interesting applications especially for the low-cost metrology applications that can now use a simple micro-controller for the complete data acquisition and signal processing. Another advantage is the easy scalability to other multiport systems or dual Six-Port configurations that feature a higher number of baseband signals. However, the phase correction filters add an additional time delay between target movement and a corresponding measurement result. Each channel has to pass a $N = 55$ lowpass-filter running at f_s. With the group delay of a linear phase FIR filter being $N/2$ and a channel sampling rate $f_s = 2$ kSa/s this leads to a time delay of 13.75 ms due to the phase correction. Especially for closed-loop systems and real-time critical applications it is desirable to keep this number as low as possible.

VI. CONCLUSION

Due to their simple passive structure and high phase resolution Six-Port interferometers are often addressing low-cost applications. This paper showed the applicability of a digital phase correction technique when using only a single multiplexed ADC instead of one each per baseband channel. A system demonstrator with a cheap and low-power 16-bit micro-controller was shown that completely integrates the signal acquisition and correction processing with a measurement update rate of up to 2000 Hz based on an efficient polyphase implementation.

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